The Engineer's Guide To EMI In DC-DC Converters (Part 10): Input Filter Impact On Stability

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Complying with regulations designed to limit conducted electromagnetic interference (EMI) usually requires the insertion of a low-pass EMI filter between a switching power converter and its source. Part 2 of this EMI article series[1-9] provided a detailed perspective of noise propagation and the requirement for both differential-mode (DM) and common-mode (CM) input filtering as an essential part of switching power-supply design. However, dynamic interactions may occur due to a poorly damped EMI filter subsystem when connected to a regulated dc-dc converter. Here in part 10, the interaction between EMI filter and dc-dc converter is addressed including its impact on overall system stability and transient performance.

Stability degradation may occur when an input filter is connected to one or more switching converters. A converter with tight feedback regulation behaves as a constant-power load at its input terminals within its control-loop bandwidth and exhibits so-called negative incremental input impedance.[10, 11] This characteristic is notorious for leading to undesirable destabilizing effects and deteriorating critical performance-related transfer functions of the converter.[12-18]

Of particular importance is peaking of the input filter's output impedance due to the high-Q parallel resonant behavior of the filter components, where impedance overlap with the converter input impedance can occur over a certain frequency range. The DM filter stage is typically most relevant, especially when using ceramic capacitors; however, the CM noise propagation path also has high-Q characteristics due to a lack of parasitic power loss in the CM noise propagation path. Passive damping of the filter is usually required to confine its output impedance peaking behavior, thus providing robust stability and unaffected transient performance.

Following an analysis of cascaded systems and the impact of impedance interaction dynamics on stability, this article presents simulation results using a synchronous buck controller with voltage-mode control to illustrate the important characteristics of the stability criteria.

General Stability Criteria For Cascaded Systems

CalTech professor David Middlebrook established the foundation of impedance-based stability and transient-performance analyses in 1976 when he published his input filter design rules[10] for a regulated converter in continuous conduction mode (CCM). Since then, the "minor-loop gain" comprising the internal impedances of the source and load subsystems has been used extensively to assess the small-signal stability of interconnected systems.[11-13] Consider a general case where two individually stable subsystems are cascaded, as shown in Fig. 1.
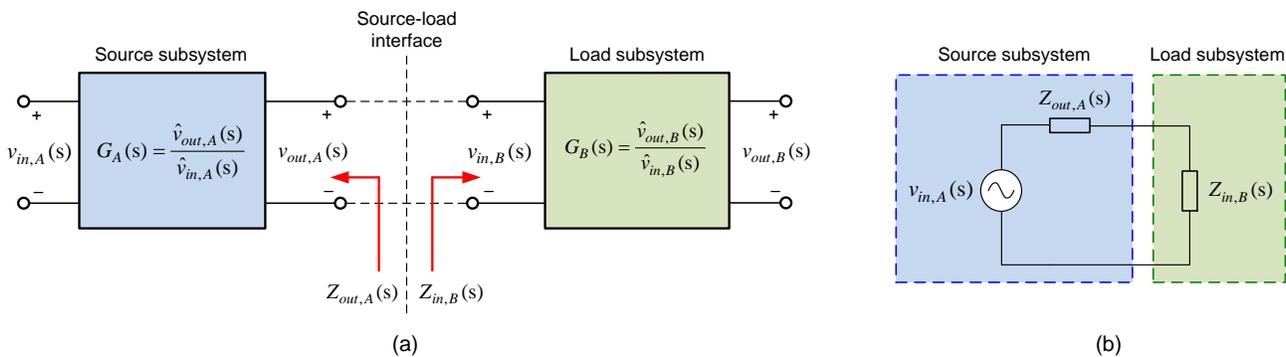

Fig. 1. Cascaded connection of two stable and independent subsystems (a) and a simplified small-signal diagram showing the loading effect on source subsystem by load subsystem (b).

Equations 1 and 2 define the small-signal input-to-output transfer function of the cascaded system and the minor-loop gain, respectively:

$$\frac{\hat{v}_{out,B}(s)}{\hat{v}_{in,A}(s)} = G_A(s)G_B(s)\frac{Z_{in,B}(s)}{Z_{in,B}(s)+Z_{out,A}(s)} = \frac{G_A(s)G_B(s)}{1+T_M(s)} \qquad (1)$$

$$T_M(s) = \frac{Z_{out,A}(s)}{Z_{in,B}(s)} \qquad (2)$$

where $Z_{out,A}(s)$ is the output impedance of the upstream subsystem and $Z_{in,B}(s)$ is the input impedance of the downstream subsystem.

Since $G_A(s)$ and $G_B(s)$ are standalone-stable small-signal transfer functions, the multiplication factor $1/[1+T_M(s)]$ represents the effect of interaction between the two subsystems. The minor-loop gain $T_M(s)$ is an impedance ratio used to assess the state of stability of the interconnected system. Interconnecting the source and load subsystems adds more poles to the overall system due to the added $(1+T_M(s))$ term, which alters the system's overall dynamic response.

It is possible to obtain a *necessary* and *sufficient* condition for system stability by applying the Nyquist criterion to the minor-loop gain. The interconnected system is stable if the Nyquist contour of $T_M(s)$ does not encircle the (−1, 0) point in the complex plane. Equivalently, the characteristic polynomial $1/[1+T_M(s)]$ should meet the Routh-Hurwitz criterion so that the system does not have right-half-plane poles.

The Middlebrook criterion given by equation 3 goes a step further and specifies, quite conservatively, that the system is stable if the minor-loop gain is such that $\left|Z_{out,A}(s)\right| \ll \left|Z_{in,B}(s)\right|$ over all frequencies. As such, this design condition is sufficient but not necessary for stability. A violation does not necessarily result in instability, as the phase may not be less than 180 degrees when the impedances overlap.

$$\left|T_M(s)\right| = \left|\frac{Z_{out,A}(s)}{Z_{in,B}(s)}\right| \ll 1 \quad \Rightarrow \quad \left|Z_{out,A}(j\omega)\right| \ll \left|Z_{in,B}(j\omega)\right| \ \forall\,\omega \qquad (3)$$

Of course, this conservativeness is consistent with the idea of providing a margin of stability. Fig. 2a shows a minor-loop-gain plot[15] that indicates an unstable system as the magnitude exceeds unity with the phase below -180 degrees. Note that Middlebrook's criterion depends on impedance magnitudes only, which makes this a convenient design-oriented criterion. Fig. 2b shows the concept of a forbidden region in the complex plane by confining the Nyquist contour of $T_M(s)$ inside the unit circle such that encirclement of the (−1, 0) point cannot occur.
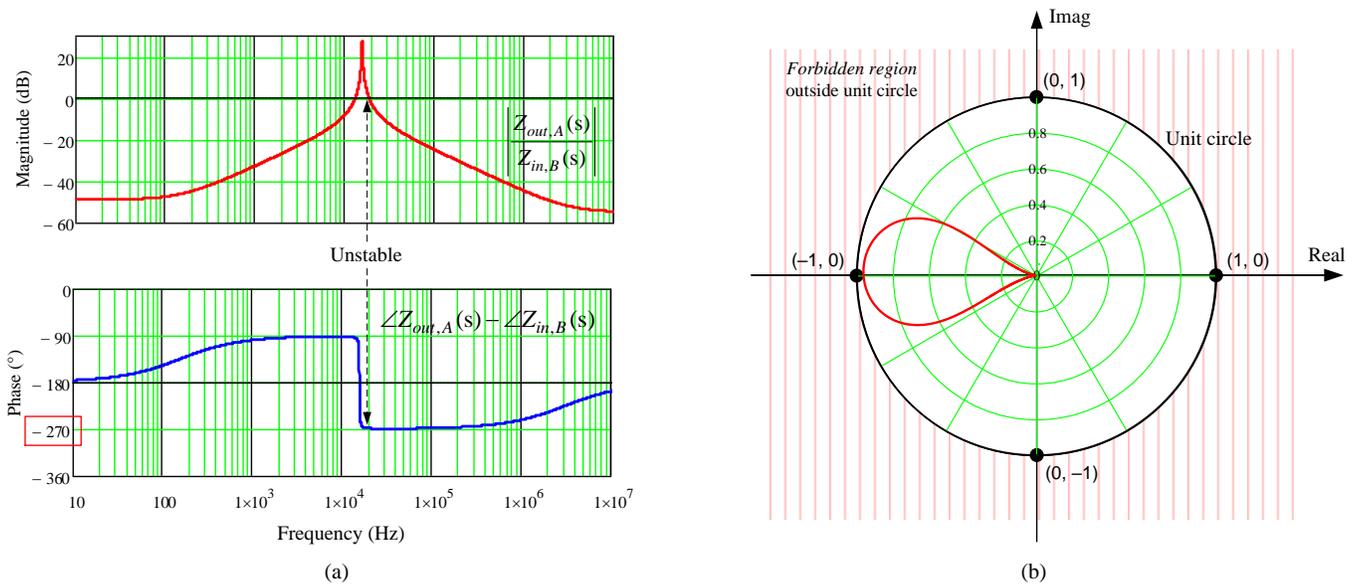
Fig. 2. Bode plot of minor-loop gain demonstrating an unstable system (a) and Nyquist plot of a stable system with a forbidden region denoted by the hatched area outside the unit circle (b).

Middlebrook suggested a practical design rule set by equation 4 such that the resulting Nyquist plot of the minor-loop gain must always lie inside a circle with a radius equal to the inverse of the desired gain margin (GM). This sets a forbidden region for $T_M(s)$ that is the outside of the circle centered at (0, 0) with radius $1/GM$.

$$\left| T_M(s) \right| = \left| \frac{Z_{out,A}(s)}{Z_{in,B}(s)} \right| = \frac{1}{GM} \quad \text{with} \quad GM > 1 \qquad (4)$$

To relax the conservativeness imposed by the Middlebrook criterion and define a more moderate impedance specification, other sources have proposed design-oriented criteria.[14] Some design criteria also seek to expand the approach to cover a load system that consists of multiple load modules, such as in a distributed power architecture with an upstream intermediate bus converter feeding numerous downstream point-of-load converters. Several such criteria are illustrated in the Nyquist plot of Fig. 3, with the forbidden regions denoted by arrows (that is, outside the red circle for the Middlebrook criterion and to the left of the applicable boundaries for the other criteria).
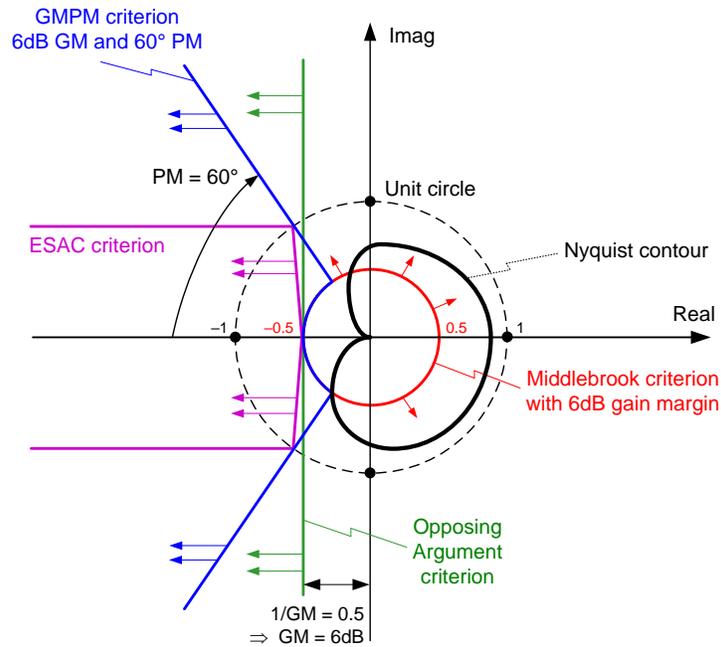
Fig. 3. Various criteria—gain margin phase margin (GMPM) (blue), opposing argument (green) and ESAC (purple)—define a system stability margin requirement more lenient than that proposed by Middlebrook (red).

As an example, the GMPM criterion sets a forbidden region as shown in equation 5:

$$\left| Z_{out,A}(s) \right| - \left| Z_{in,B}(s) \right| > \text{GM}$$

$$\left| \angle Z_{out,A}(s) - \angle Z_{in,B}(s) \right| > 180° - \text{PM}$$

(5)

As illustrated by the blue lines in Fig. 3, by keeping out of this forbidden region with a GM of 6 dB (a circle radius of 0.5) and a phase margin (PM) of 60 degrees, small-signal system stability will keep the system from being conditionally stable.

Impact Of Input Filter On Converter Stability

Now let's consider the specific case represented in Fig. 4 for the stability of a feedback-controlled dc-dc converter affected by the addition of an input filter.

(a)

$$\hat{v}_{in,C}(s) = \hat{v}_{in}(s) \frac{Z_{in,C}(s)}{Z_{in,C}(s) + Z_{out,F}(s)} = \frac{\hat{v}_{in}(s)}{1 + \dfrac{Z_{out,F}(s)}{Z_{in,C}(s)}} = \frac{\hat{v}_{in}(s)}{1 + T_M(s)}$$
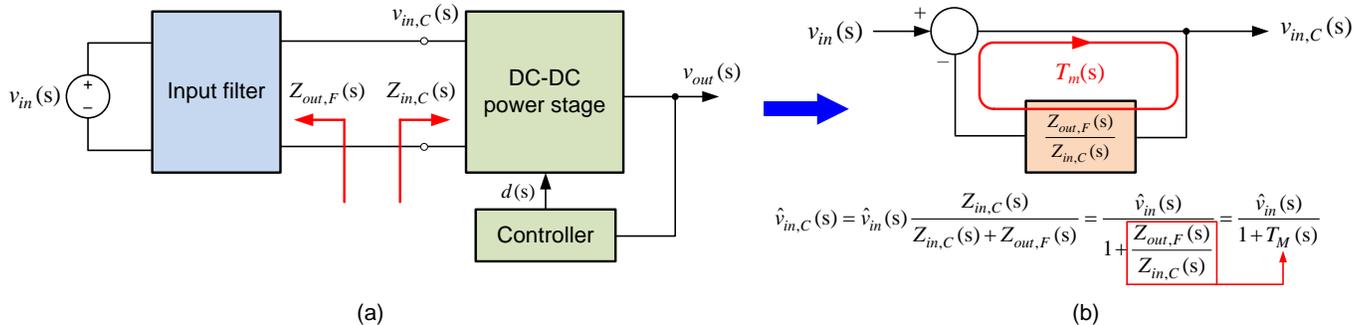
(b)

Fig. 4. Functional block diagram of an EMI input filter stage and feedback-controlled switching converter (a) and the equivalent feedback minor loop (b).

By defining $Z_{out,F}(s)$ as the Thevenin output impedance of the filter and $Z_{in,C}(s)$ as the input impedance of the converter, you can obtain the small-signal transfer function of the interconnected system through equations 6 and 7:

$$\frac{\hat{v}_{in,C}(s)}{\hat{v}_{in}(s)} = \frac{Z_{in,C}(s)}{Z_{in,C}(s) + Z_{out,F}(s)} = \frac{1}{1 + \dfrac{Z_{out,F}(s)}{Z_{in,C}(s)}} = \frac{1}{1 + T_M(s)} \qquad (6)$$

$$T_M(s) = \frac{Z_{out,F}(s)}{Z_{in,C}(s)} \qquad (7)$$

Dynamic coupling between the EMI filter and the converter effectively creates a feedback loop (see Fig. 4b). Taking into account the individual impedances at the interface as seen from the converter input terminals determines the stability of the cascaded system. Equation 7 defines the minor-loop gain as the ratio of the output impedance of the filter to the closed-loop input impedance of the converter.

As expressed by equation 8, the Middlebrook criterion gives a simple design-oriented condition for stability by limiting the magnitude of the minor-loop gain[10-12] over the entire frequency range:

$$\left| T_M(s) \right| = \left| \frac{Z_{out,F}(s)}{Z_{in,C}(s)} \right| << 1 \quad \Rightarrow \quad \left| Z_{out,F}(j\omega) \right| << \left| Z_{in,C}(j\omega) \right| \ \forall \omega \quad (8)$$

If $Z_{in,C}(s)$ is known, a practical design rule for $Z_{out,F}(s)$ set by equation 9 requires that the resulting minor-loop gain always lie inside a circle with a radius equal to the inverse of the desired GM. As previously outlined, this defines a forbidden region for $T_M(s)$ in the complex plane that is the outside of the circle centered at (0, 0) with radius 1/GM.

$$\left| T_M(s) \right| = \left| \frac{Z_{out,F}(s)}{Z_{in,C}(s)} \right| = \frac{1}{GM} \qquad (9)$$

While the closed-loop input impedance alone is not sufficient to prove that the input filter does not impact the dynamic performance of the converter, it is a sufficient check for system stability. The issue of dynamic interaction effects on system transient performance can be explicitly addressed using Middlebrook's Extra Element Theorem (this will be examined in a subsequent part of this article series). The following two sections provide additional context for $Z_{out,F}(s)$ and $Z_{in,C}(s)$.

Output Impedance of the EMI Filter, $Z_{out,F}(s)$

Fig. 5a shows the small-signal output impedance measurement by injecting a test current into a single-stage LC filter and measuring the resulting voltage. The filter inductance and its dc resistance (DCR) can assimilate a connection impedance from the source to the filter, described by a parasitic inductance L_s and a resistance R_s, as they effectively appear in series. Equation 10 provides the expression for the output impedance, which is plotted in Fig. 5b as a parallel resonant characteristic:

$$Z_{out,F}(s) = \left(r_L + sL_f \right) \Big\| \left(r_C + \frac{1}{sC_f} \right) = r_L \frac{\left(1 + s\dfrac{L_f}{r_L} \right)\left(1 + sr_C C_f \right)}{1 + sC_f \left(r_L + r_C \right) + s^2 L_f C_f} \qquad (10)$$

Equation 11 expresses this in a standardized form and identifies a complex pole pair and two real zeros. If the filter capacitance is a ceramic with low equivalent series resistance (ESR) instead of a high-ESR electrolytic, and the filter inductor has low DCR, then the output impedance has a high Q-factor and peaking effect.

$$Z_{out,F}(s) = r_L \frac{\left(1 + \dfrac{s}{\omega_{z1}}\right)\left(1 + \dfrac{s}{\omega_{z2}}\right)}{1 + \dfrac{s}{\omega_o Q} + \dfrac{s^2}{\omega_o^2}}, \quad \text{where} \quad \begin{cases} Q = \dfrac{R_o}{r_L + r_C} \quad R_o = \sqrt{\dfrac{L_f}{C_f}} \quad \omega_o = \dfrac{1}{\sqrt{L_f C_f}} \\ \\ \omega_{z1} = \dfrac{r_L}{L_f} \quad \omega_{z2} = \dfrac{1}{r_C C_f} \end{cases} \tag{11}$$

It is possible to apply a similar measurement procedure for a π-filter or a two-stage EMI filter. The last stage of a multistage filter, typically responsible for filtering of the switching frequency and lower-order harmonics, usually dominates the filter output impedance.
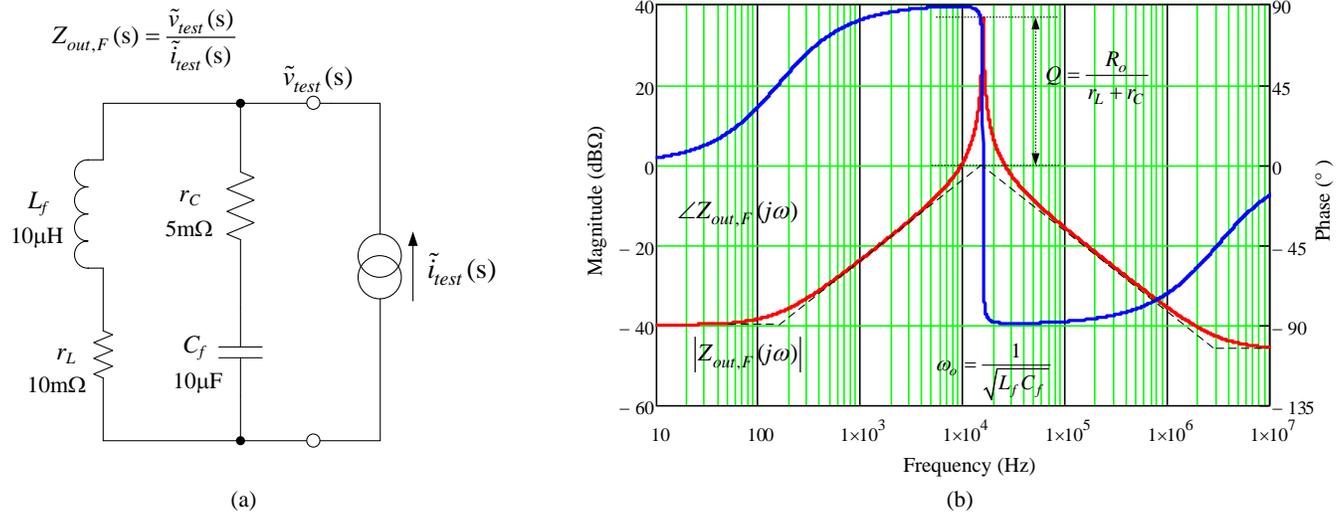

(a)   (b)

*Fig. 5. Injection of a test current in the single-stage LC filter (with its input port shorted) (a)
permits calculation of its output impedance, for which magnitude and phase are plotted in (b).*

Closed-Loop Input Impedance Of A DC-DC Converter, $Z_{in,C}(s)$

As I mentioned earlier, the feedback loop of a regulated dc-dc converter acts to set the output power of the converter instantaneously constant, rejecting input voltage variations and hence making the converter input port appear as a constant-power load (CPL). Fig. 6 shows a CPL characteristic and its linearization about a quiescent operating point.
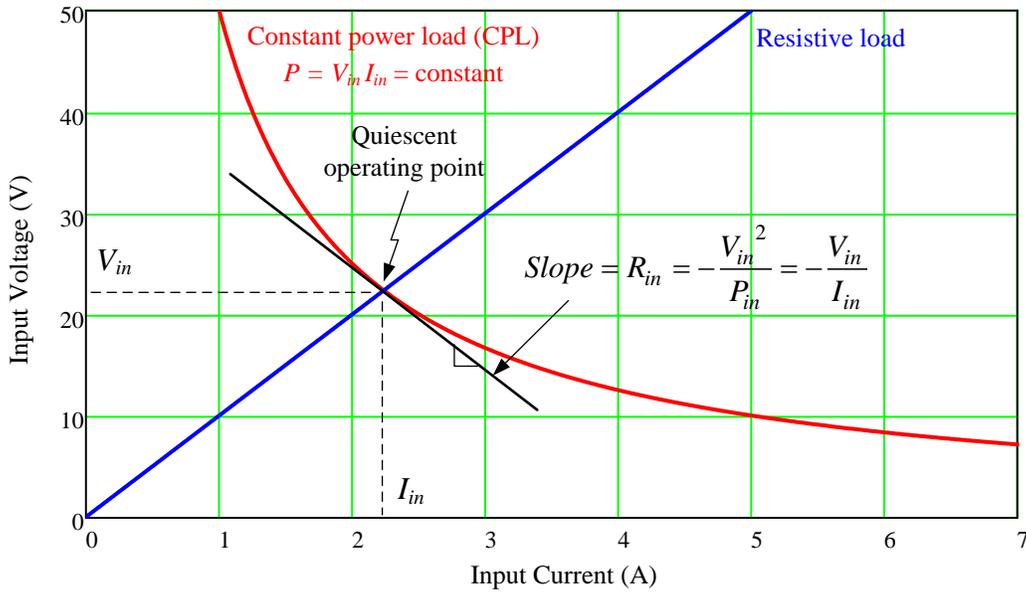
Fig. 6. V-I behavior of a conventional resistive load versus a CPL.

The negative slope at the quiescent operating point implies a phase of -180 degrees and thus a negative incremental resistance. As a result, when a lightly damped input filter is connected to a converter input port, the input filter can interact with the negative impedance characteristic to establish a negative resistance oscillator.[15-18] Equation 12 derives the small-signal input resistance about a quiescent operating point:

$$\frac{\partial i_{in}}{\partial v_{in}} = \frac{\partial \left(p_{out}/\eta\, v_{in} \right)}{\partial v_{in}} = -\frac{P_{out}}{V_{in}^2\, \eta} \quad \Rightarrow \quad R_{in} = -\frac{V_{in}^2\, \eta}{P_{out}} = -\frac{V_{in}}{I_{in}} = -\frac{R}{M^2}\, \eta \quad (12)$$

where $M = V_{out}/V_{in}$ is the voltage conversion ratio, R is the load resistance and η is the conversion efficiency.

Equation 13 provides the closed-loop input impedance[15-17] of a voltage-mode buck converter operating in CCM, where $D = V_{out}/V_{in}$ is the duty cycle and $L(\text{s})$ is the voltage-loop gain:

$$Z_{in,C}(\text{s}) = \left.\frac{\hat{v}_{in}(\text{s})}{\hat{i}_{in}(\text{s})}\right|_{\hat{i}_{out}(\text{s})=0} = \frac{\left[1+L(\text{s})\right]Z_{in,OL}(\text{s})}{1 - \dfrac{D^2}{R}L(\text{s})Z_{in,OL}(\text{s})}$$

$$(13)$$

$$\text{where} \quad Z_{in,OL}(\text{s}) = \left.\frac{\hat{v}_{in}(\text{s})}{\hat{i}_{in}(\text{s})}\right|_{\substack{\hat{d}(\text{s})=0 \\ \hat{i}_{out}(\text{s})=0}} = \frac{R}{D^2}\frac{1+\text{s}\dfrac{L_o}{R}+\text{s}^2 L_o C_o}{1+\text{s}RC_o}$$

Fig. 7a shows a typical plot of the closed-loop input impedance of a buck converter when measured at the switching cell input. As predicted by equation 13, the behavior corresponds to a negative resistance of $-V_{in}/I_{in}$ at low frequency, well below the converter's loop crossover frequency f_c, and above that frequency converges to the open-loop input impedance, $Z_{in,OL}(\text{s})$.

Calculated plots of $Z_{out,F}(s)$ and $Z_{in,C}(s)$ are shown in Fig. 7b, highlighting an interaction around f_{int}. Note that an impedance overlap in the low-frequency region where $f < f_c$ implies $\left|T_M(s)\right| > 1$ and $\left|\angle T_M(s)\right| > 180°$; the Nyquist plot of $T_M(s)$ will thus encircle $(-1, 0)$.
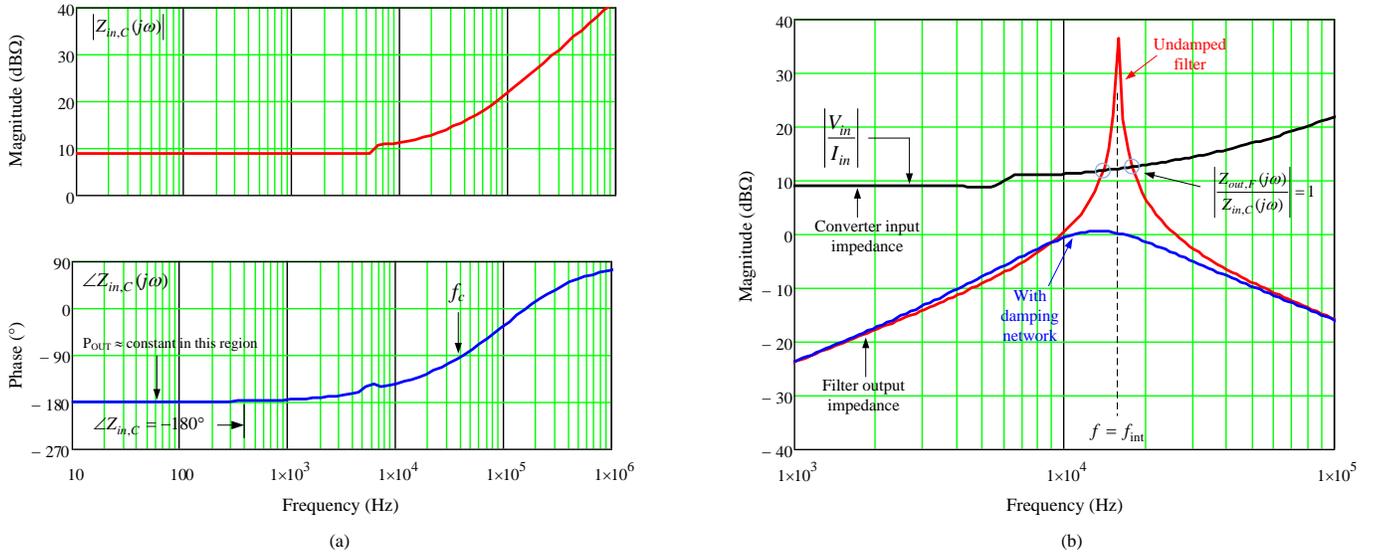

(a)

(b)

Fig. 7. Plot of closed-loop input impedance magnitude and phase (a) and impedance overlap check (b).

Checking System Stability Via Simulation

Fig. 8 shows the SIMPLIS schematic of a synchronous buck dc-dc regulator using parameters from the LM5146-Q1 voltage-mode controller[19] with line feedforward. The input voltage is 12 V and the output is 5 V at 10 A. Component selection for the type-3 compensation circuit sets the voltage-loop crossover at 40 kHz.

A single-stage LC filter connects at the input to provide DM noise attenuation. Between the filter and buck power stage is a perturbation source, similar to that used in a practical setup,[18] to measure filter output impedance and converter input impedance.
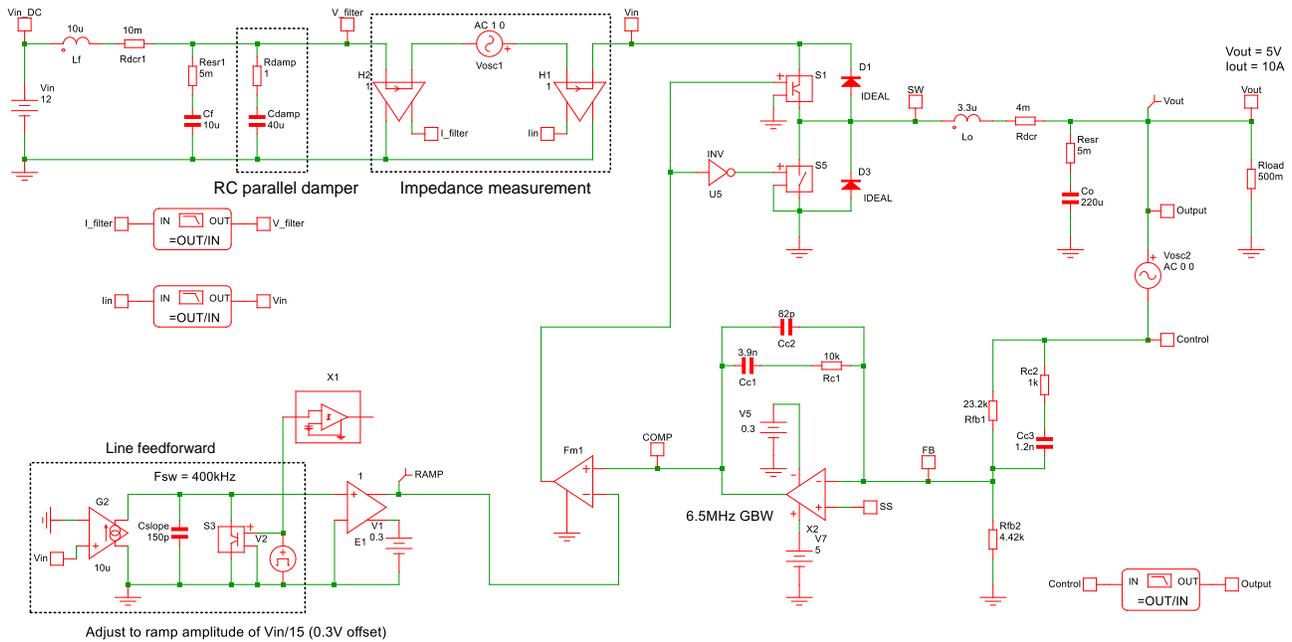
Fig. 8. SIMPLIS simulation schematic with VIN = 12 V, VOUT = 5 V and IOUT = 10 A.

Fig. 9 shows the impedance behavior with and without an RC parallel damping circuit connected across the input filter capacitor, Cf. The damping capacitance is set at four times that of Cf, and the damping resistance is equal to the filter characteristic impedance given by equation 11. Whereas the undamped filter output impedance exceeds the converter input impedance by 25 dB at minimum input voltage, the damped characteristic provides 9 dB of margin.
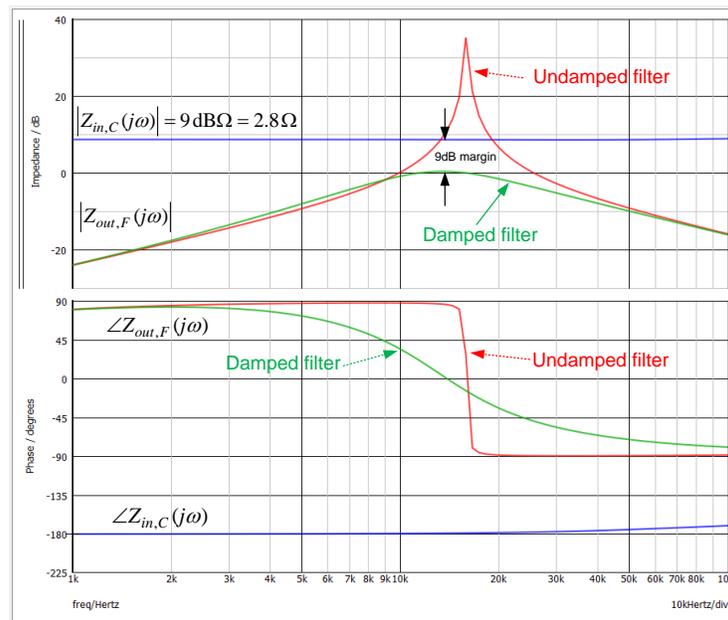

Fig. 9. SIMPLIS simulation of regulator input impedance and filter output impedance with and without an RC parallel damper connected.

Depending on the bandwidth of the line-feedforward amplifier, the voltage-mode controller provides high input-to-output attenuation.[20] This also enables a flat closed-loop input impedance characteristic and a phase of -180 degrees extending to a much higher frequency than that shown in Fig. 7.

Also noteworthy is that the input to the switching cell is the point at which the interaction analysis is properly applied to predict whether the input filter affects the control loop. However, the component grouping in most practical situations is such that some of the input filter components are in parallel with the input of the power supply (for example, the input capacitor of a buck converter). This can lead to false-low measurements that are not valid per Middlebrook's original discussions.[18]

Summary

A methodology for analyzing input filter interaction has long been established by Middlebrook to show how the EMI input filter stage can alter the stability of a switching power converter. The minor-loop gain defines the ratio of the input-filter output impedance and the closed-loop input impedance of the converter by means of which the system stability can be determined by applying the Nyquist stability criterion. In general, the EMI filter must be sufficiently damped so that the EMI-filter output impedance peak is much less than the closed-loop converter input impedance.

While the filter configurations used to meet conducted emissions standards may be more complex than the simple LC filter discussed here, a similar damping network applies, and the measurement technique remains the same. Many power-supply designers underestimate the space consumed by a damping network or, quite often, completely overlook the necessity for input-filter damping.

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For more information on EMI, see How2Power's Power Supply EMI Anthology. Also see the How2Power's Design Guide, locate the Design Area category and select "EMI and EMC".