Flyback Magnetics: Winding-Current Transition Is Key To Efficiency

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Flyback converters are isolated PWM-switch common-inductor (CL) configured converters, and a common power supply design choice at low power (<100 W). This article presents, with derivations, the design formulas that apply to flyback converter coupled inductors as part of the magnetics design of the converter.

After a brief review of flyback circuit operation and the role of the coupled inductors, the design of the coupled inductors or *transductor*, is discussed at length. First, a primary-side-referred model of the transductor is described and tranductor operation during flyback is explained further. Next, the choice of the clamp voltage V_{CL} is discussed with attention to its impact on the primary-to-secondary current transfer delay time t_d and that parameter's effect on converter efficiency.

The role of these parameters is further illuminated in the description that follows of current transfer from primary to secondary winding. Finally a transductor model is presented that describes the current transfer during t_d.

Flyback Operation

A basic flyback converter is shown in Fig. 1.

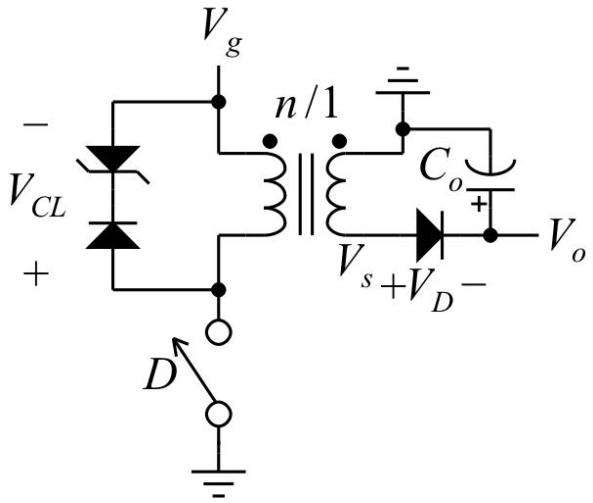

Fig. 1. Basic flyback converter, with active switch closed during on-time, $D{\cdot}T_s$, input power port at voltage, V_g and output port at $V_o = V_s - V_D$.

During the on-time interval, the active switch conducts and flux increases in the primary winding of the transductor (in this case, a two-winding inductor). The voltage across the secondary winding is positive at the dotted terminal and the secondary diode is off. When the switch opens, primary current flows into the diode clamp with opposing voltage, V_{CL} while magnetizing current transfers to the secondary winding. Thus, the transductor functions as a coupled inductor, not a transformer. If the winding coupling is high ($k \approx 1$) the transfer occurs quickly and little power is dissipated in the clamp, from leakage-inductance loss.

The per-cycle power of the transductor transfers to the output during the off-time at an average secondary winding voltage amplitude of V_s, with no output transfer from V_g. Thus, this is a PWM-switch common-inductor (CL) configuration with magnetic isolation. The simplified transfer equation can be derived by assuming steady-state operation and flux balance in the inductor with perfect ($k = 1$) coupling between windings;

$$\Delta\lambda = 0 \text{ V·s} \Rightarrow V_g \cdot D \cdot T_s = V_s \cdot D' \cdot T_s \Rightarrow \frac{V_s}{V_g} = \frac{D}{D'}$$

At low power, it is more difficult to achieve high efficiency because otherwise negligible power losses, such as in the control circuitry, significantly reduce efficiency. One of the main causes of power loss in flyback converters is the leakage inductance, L_l of the coupled inductor. Minimization of leakage-inductance power loss is consequently of major interest in the design of flyback converters.

Flyback Magnetics

The equivalent inductor circuit during the off-time transfer of current from primary to secondary winding is shown in Fig. 2. The primary winding inductance, L_p consists of magnetizing inductance, L_m shared mutually by the windings, in series with primary leakage inductance, L_{lp}. The secondary winding also has leakage inductance, L_{ls}. Impedances in a winding can be referred to other windings by n^2, and the amount of referral, or *referral ratio*, is arbitrary. If the referral ratio, a is the turns ratio, n ($a = n$), then leakage inductance is made the same for both windings, and

$$L_{lp} = a^2 \cdot L_{ls} = n^2 \cdot L_{ls} = L_{ls}', \; a = n$$

Turns ratio, n is usually the referral ratio encountered, though some analyses can be simplified by placing all of the leakage inductance, L_l on one or the other winding.[1] The Fig. 2 circuit combines L_{lp} and $L_{ls}' = n^2 \cdot L_{ls}$ as L_l on the primary side. (For a balanced $a = n$ model, the Fig. 2 circuit diagram would have L_{lp} in place of L_l and an addional L_{ls}' in series with V_s'.) For flyback analysis, all of L_{ls} is referred to the primary.

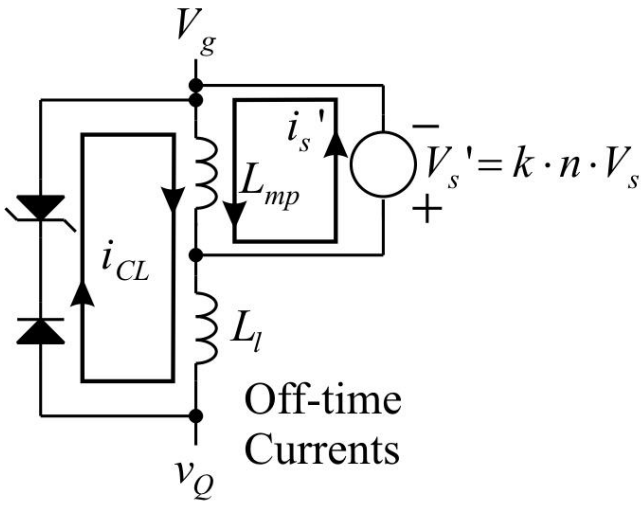

Fig. 2. Transductor-centered circuit behavior at the beginning of off-time, when current is transferring between windings. Secondary leakage inductance is referred to the primary and for both windings, combined as L_l. The secondary voltage source—the large output capacitor, C_o in Fig. 1— appears across L_{mp} as V_s' with the rectifier conducting.

Then the referral ratio becomes $a = k \cdot n$, and the combined leakage inductance is

$$L_l = (1 - k^2) \cdot L_p \text{ , primary-referred}$$

where the interwinding coupling coefficient, k is the fraction of winding inductance that is magnetizing inductance, or $L_{mp} = k \cdot L_p$. However, with $a = k \cdot n$, it becomes $L_{mp} = k^2 \cdot L_p$. The remaining L_p is primary-side leakage inductance, $L_l = (1 - k^2) \cdot L_p$. By using a instead of turns ratio, n, as the winding referral ratio, all the leakage inductance is referred to the primary side of the transductor. The equivalent circuit is shown in Fig. 3.

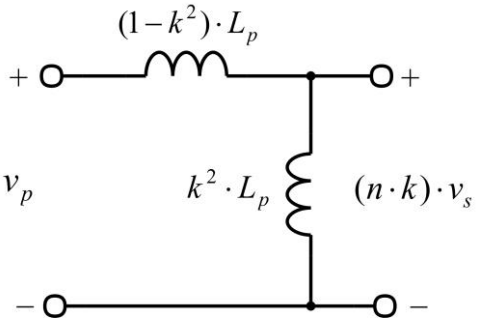

Fig. 3. Transductor model with secondary leakage inductance referred to the primary side. The referral ratio, a is no longer the turns ratio, n but is a = k·n. Combining leakage inductance into one circuit element simplifies analysis.

Leakage inductance of a winding is independent of other windings and is the same as though an external inductance were added in series with the winding. How much of each L_{lx} is referred from one winding to the other is arbitrary in the choice of *a*. Flyback analysis is simplified by referring all leakage inductance to the primary winding; then the circuit has only one leakage inductance, L_l.

The magnetizing inductance, L_m, is in the transductor field reference-frame of the core, on neither the primary nor secondary side. Winding-to-field referral of external secondary voltage, V_s is V_s/N_s, and field to primary winding voltage referral is N_p. Then the winding-to-field-to-winding referral is the product, $(V_s/N_s)\cdot N_p = n\cdot V_s$, and the turns ratio, $n = N_p/N_s$ is the result of two successive winding ⇔ field referrals. L_m is referred from the field to the primary winding circuit as L_{mp}, the magnetizing inductance across the primary terminals.

L_m couples to the secondary circuit where C_o holds the output voltage relatively constant so that it appears as a voltage source. Adding to the secondary diode drop, the secondary winding voltage refers to the primary winding, by $n\cdot k$, as the *flyback voltage*, V_s'. It is generally desirable to tightly couple the windings so that $k \approx 1$. The flyback voltage couples across the primary mutual inductance, L_{mp}, but not across the primary-referred leakage inductance, L_l.

Clamp Voltage

When the active switch (D in Fig. 1) shuts off, the current in both inductances will continue to flow somewhere. The current in L_{mp} diverts to the secondary circuit (referred to the primary) and flows into the V_s' source (of C_o), with current decreasing at the rate of $-V_s'/L_{mp}$. With the active switch off, the current through L_l has nowhere to go other than into the diode clamp.

The voltage across L_l is the clamp voltage, V_{CL} minus V_s'. If the turns ratio, $n = N_p/N_s = 8$, $k = 0.99$, and

$$V_s = V_D + V_o = 0.8\text{ V} + 5.0\text{ V} = 5.8\text{ V} \;\Rightarrow V_s' = k\cdot n\cdot V_s \approx (0.99)\cdot 8\cdot(5.8\text{ V}) = 45.94\text{ V}$$

To deflux the leakage inductance quickly (for efficient current transfer to the secondary), the opposing voltage of the clamp across L_l must be $V_{CL} > V_s' \approx V_g$. To choose a clamp voltage for clamp design, the transfer time, t_d of the primary current to the secondary winding is a major consideration.

Suppose the primary inductance is 1 mH and the coupling coefficient of the transformer is $k = 0.99$. Then

$$L_l = (1 - k^2)\cdot L_p = (0.02)\cdot(1\text{ mH}) = 20\ \mu\text{H}$$

If the converter switching frequency is 200 kHz, then the switching period is $T_s = 5\ \mu$s. The primary-to-secondary current transfer delay time, t_d , is solved from

$$\frac{V_{CL} - V_s'}{L_l} = \frac{\hat{i}_p}{t_d} \;\Rightarrow\; t_d = L_l \cdot \frac{\hat{i}_p}{V_{CL} - V_s'}$$

where for DCM, $i_p(0\text{ s}) = \Delta i_p = \hat{i}_p$.

A flyback design goal is to maximize transfer efficiency by minimizing t_d to be a small fraction of T_s. Additionally, in the inductor design, L_l is minimized by achieving the tightest coupling—that is, by maximizing k. A per-cycle peak-current (current-mode) controller has a peak primary current determined by the circuit. The turns ratio is set by optimizing the duty ratio over the input voltage and load current ranges. This sets V_s'. Transductor design determines L_l. The only choice remaining is clamp voltage, V_{CL}. The higher V_{CL} is made, the shorter is t_d.

Component voltage ratings—especially that of the power switch—limit the choice of how high V_{CL} can be made. Rated switch voltage must exceed $V_{CL} + V_g$ for maximum V_g. Commercially available avalanche diodes of the 1 W to 5 W range are also limited in upper voltage range to about 200 V, but usually must be kept below 50 V by power limitations.

To illustrate, assume the peak primary current, $\hat{i}_p$ = 0.25 A. Then transfer delay time can be calculated given various values of clamp voltage. For V_{CL} = 60 V, t_d = 356 ns, or about 7.1% of the switching period. By increasing clamp voltage to 100 V,

$$t_d = 20\,\mu\text{H} \cdot \frac{0.25\,\text{A}}{100\,\text{V} - 45.94\,\text{V}} = 92.5\,\text{ns}$$

or 1.85% of the switching period. Commercial 100-V avalanche diodes tend to be expensive and have limited current ratings. A 0.4-W, 100-V component is limited to an rms current of 4 mA. Current at 0.25 A for 1.85% of the time is about 4.62 mA rms. Diode power requirements can make their use suboptimal.

Current Transfer

The current transfer waveforms are shown in Fig. 4. Primary current transfers to the secondary winding during transfer interval, t_d, as shown. The slopes of the current ramps of the two waveforms are derived from the inductor v-i relationship, $V/L = \Delta i/\Delta t$ for current ramps. V_g is applied to L_p during on-time, t_{on}, the time the active switch conducts. Primary current peaks at the end of on-time at

$$\hat{i}_p = \frac{V_g}{L_p} \cdot t_{on}\ ,\ t_{on} = D \cdot T_s$$

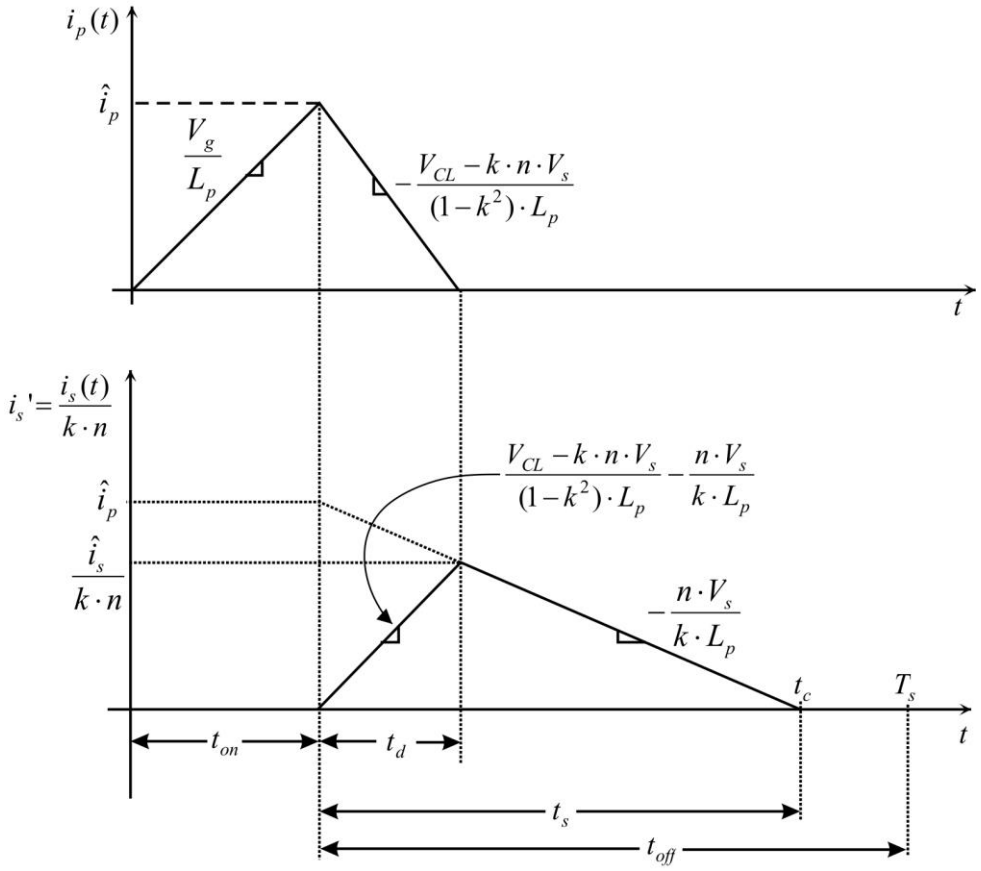

Fig. 4. Flyback current waveforms, emphasizing the winding current transfer detail.

The secondary-circuit diode is reverse-biased and no secondary current flows during on-time. When the switch opens, both clamp and secondary current conduct during transfer time, t_d. The secondary circuit refers the output voltage plus rectifier diode drop, $V_o + V_D = V_s$ as the secondary winding voltage to the primary by the referral ratio, $k{\cdot}n$ as $V_s' = k{\cdot}n{\cdot}V_s$. This flyback voltage is applied across the mutually-coupled part of the primary winding, $L_{mp} = k^2{\cdot}L_p$, as shown in the circuit diagram of Fig. 2.

The secondary current referred to the primary, is $i_s/k{\cdot}n \approx i_s/n$, and is plotted as $i_s'(t)$ on the lower graph of Fig. 4. The waveforms show that the converter is operating DCM because the secondary current becomes zero at t_c, before the end of the cycle. ($t_c < T_s \Rightarrow$ DCM) The *conduction duty-ratio* for DCM operation is

$$D_c = \frac{t_c}{T_s}$$

The primary-side clamp current ramps down at a rate determined by the voltage across the leakage inductance, $L_l = (1 - k^2){\cdot}L_p$. This voltage is the difference between the clamp voltage, V_{CL}, and the flyback voltage, V_s'. From this, the transfer time is

$$t_d = \frac{-\hat{i}_p}{-\frac{V_{CL}-k\cdot n\cdot V_s}{(1-k^2)\cdot L_p}} = \frac{(1-k^2)\cdot L_p}{V_{CL}-k\cdot n\cdot V_s}\cdot \hat{i}_p$$

In the lower plot of Fig. 4, during t_d , i_p decreases from its peak, $\hat{i}_p$ at the primary-referred i_s′ rate until the end of t_d where $\hat{i}_s' < \hat{i}_p$. i_s′ ramps up to $\hat{i}_s'$ at the clamp-current rate (from the upper plot) minus the rate of $V_s'/k^2 \cdot L_p$, which is the ramp-down rate of i_s′. The two slopes subtract as shown in the up-slope expression on the lower plot.

Because the finite transfer time causes $\hat{i}_s'$ to be less than it would be for instantaneous transfer, it is advantageous to minimize t_d. This lost current is, in effect, retained on the primary side and the associated power dissipated in the clamp. In other words, by the time the secondary current ramps up to its peak, the secondary-current decay rate has reduced it to less than $k \cdot n \cdot \hat{i}_p$. The actual peak secondary current, referred to the primary, is

$$\hat{i}_s' = \frac{\hat{i}_s}{k \cdot n} = \left(\frac{V_{CL} - k \cdot n \cdot V_s}{(1-k^2) \cdot L_p} - \frac{n \cdot V_s}{k \cdot L_p} \right) \cdot t_d$$

$$= \hat{i}_p \cdot \left[1 - \left(\frac{1-k^2}{k} \right) \cdot \left(\frac{k \cdot n \cdot V_s}{V_{CL} - k \cdot n \cdot V_s} \right) \right] = \hat{i}_p \cdot (1-\alpha)$$

where, the $\hat{i}_p$ loss factor, (1- α) is the fraction of i_p transferred to i_s ;

$$\alpha = \left(\frac{1-k^2}{k} \right) \cdot \left(\frac{k \cdot n \cdot V_s}{V_{CL} - k \cdot n \cdot V_s} \right)$$

where α depends on k, V_s, n, and V_{CL}. Usually, $k \approx 1$, and V_s′ and n are determined by V_o and power-circuit optimization. Consequently, V_{CL} is the controlling variable for $\hat{i}_s'$. In minimizing t_d by maximizing V_{CL}, α is minimized.

The Magnetics Of Current Transfer

During the transition interval, t_d, the more detailed primary-referred transductor behavior is shown in Fig. 5.

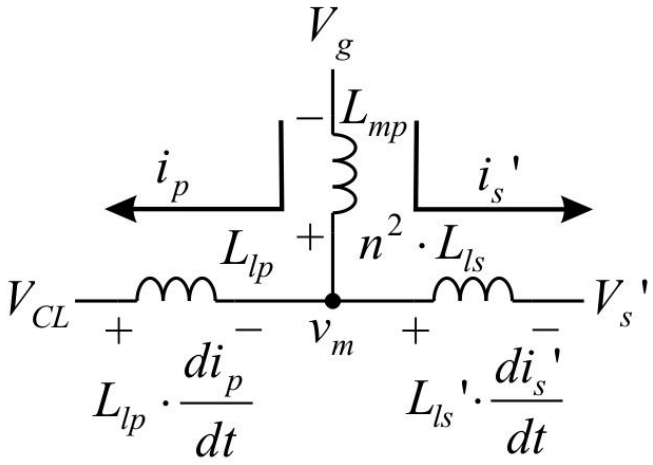

Fig. 5. Transductor model for current transfer with primary-referred primary and secondary leakage inductances separated, to show flow of currents through each and their voltages.

The voltage across the magnetizing inductance, L_{mp} is $v_m - V_g$, where v_m is the internal-node voltage of the transductor. The magnetizing current, $i_{mp} = i_p + i_s'$ splits between windings and as i_p decreases, i_s' must increase for equal leakage inductances, $L_{lp} = L_{ls}'$, at rates from the above plots;

$$\frac{di_s'}{dt} = -(1-\alpha)\cdot\frac{di_p}{dt} \; ; v_m \approx (V_{CL} + V_s')/2 \; , \; t \le t_d$$

Conclusion

In conclusion, a finite time is required for flyback current to transfer completely from primary to secondary winding. This time is affected mainly by the one free design variable, the clamp voltage, V_{CL}. The higher V_{CL} is, the higher is $\hat{i}_s$ and the higher must be the switch voltage rating, $V_{CL} + V_g$. The transfer efficiency can be assessed either by transfer time, t_d which must be short relative to the switching period, T_s or by the loss factor, α. Expressions for both are the central clamp design equations.

Reference

For more explanation of magnetic-component equivalent circuits, see the chapter, "Transductors" in Power Magnetics Design Optimization, www.innovatia.com. Purchase a paper copy of *PMDO* or request a free PDF copy through innovatia dot com/Inquiry.

About The Author

Dennis Feucht has been involved in power electronics for 30 years, designing motor-drives and power converters. He has an instrument background from Tektronix, where he designed test and measurement equipment and did research in Tek Labs. He has lately been working on projects in theoretical magnetics and power converter research.

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