B2A Series

1.80W & 2.25W DC/DC converter

B2A DC-DC Converters are typically used in point of load (POL) applications with stable loads.

- Input/output Isolation.
- Encapsulated design.

Figure 1: SCHEMATIC

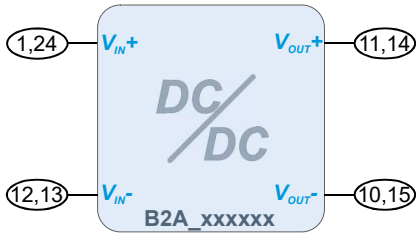


Figure 2: MECHANICAL SPECIFICATIONS (mm)

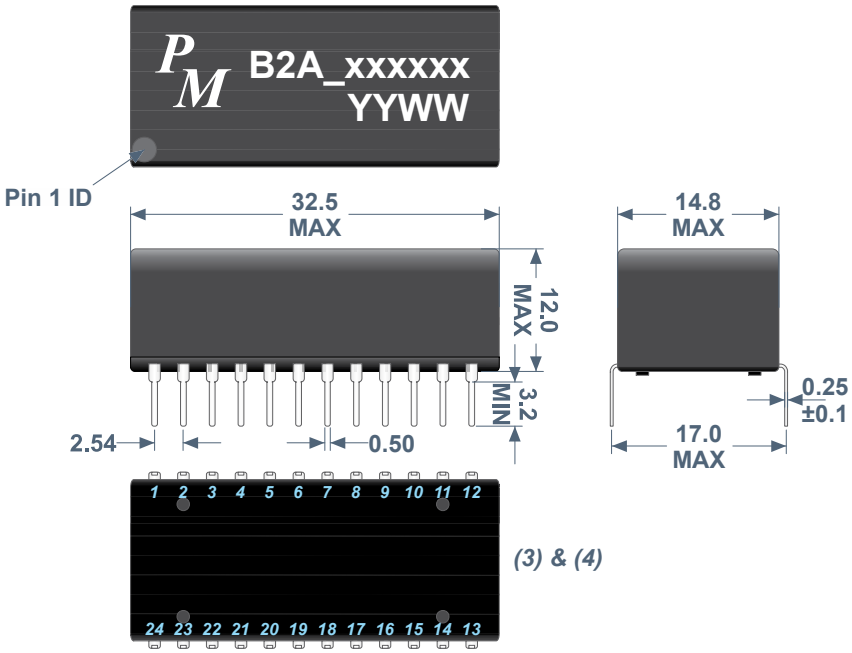


Table 1: PART NUMBER LIST. **Non-regulated Vo**

PART NUMBER	V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)
B2AU050920	5.0	480	9.0	200	1.80
B2AU050921(4)	5.0	480	9.0	200	1.80
B2AU050925	5.0	600	9.0	250	2.25
B2AU050926(4)	5.0	600	9.0	250	2.25
B2AU120920	12.0	200	9.0	200	1.80
B2AU120925	12.0	250	9.0	250	2.25

Table 2: PART NUMBER LIST. **Regulated Vo**

PART NUMBER	V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)
B2AR050920	5.0	600	9.0	200	1.80
B2AR050925	5.0	750	9.0	250	2.25
B2AR120920	12.0	250	9.0	200	1.80
B2AR120925	12.0	315	9.0	250	2.25

FEATURES:

1) Operating temperature -25°C to +70°C.
2) Storage temperature -55°C to +125°C.
3) Removed pin 4 for all part numbers.
4) Removed pins 2 through 9, and 16 through 23 for B2AU050921 and B2AU050926.
5) I_{IN} is TYP.
6) I_{OUT} is MAX.

20381 Barents Sea Circle, Lake Forest, CA 92630. ♦ Phone: 949-452-0511 ♦ E-mail: sales@premiermag.com ♦ www.premiermag.com

Table 3: ELECTRICAL SPECIFICATIONS 25°C. **Non-regulated Vo**, V_{IN}=Table 1, C_{IN}=open, C_{OUT}=open, unless otherwise noted.

PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT VOLTAGE	100%I_{OUT}	V_{IN}-10%	V_{IN}	V_{IN}+10%	V
INPUT CURRENT	0%I_{OUT}.	20	100	-	mA
OUTPUT VOLTAGE ACCURACY	100%I_{OUT}.	-5.0	-	5.0	%
OUTPUT VOLTAGE RIPPLE AND NOISE	20MHz BW, C_{OUT}= 100nF ceramic; 100%I_{OUT}.	-	-	100	mVp-p
OUTPUT VOLTAGE LINE REGULATION	From V_{IN}MAX to V_{IN}MIN; 100%I_{OUT}.	-	1.2	-	% / 1%V_{IN}
OUTPUT VOLTAGE LOAD REGULATION	From 100%I_{OUT} to 10%I_{OUT}.	-10	-	10	%
EFFICIENCY	100%I_{OUT}.	65	80	-	%
HIPOT	1,12,13,24 to 10,11,14,15; 0.5mA MAX, ramp 1s,dwell 1s.	500	-	-	V_{DC}
WEIGHT		-	9.3	-	g

Table 4: ELECTRICAL SPECIFICATIONS 25°C. **Regulated Vo**, V_{IN}=Table 2, C_{IN}=open, C_{OUT}=open, unless otherwise noted.

PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT VOLTAGE	100%I_{OUT}	V_{IN}-10%	V_{IN}	V_{IN}+10%	V
INPUT CURRENT	0%I_{OUT}.	30	120	-	mA
OUTPUT VOLTAGE ACCURACY	100%I_{OUT}.	-5.0	-	5.0	%
OUTPUT VOLTAGE RIPPLE AND NOISE	20MHz BW, C_{OUT}= 100nF ceramic; 100%I_{OUT}.	-	-	100	mVp-p
OUTPUT VOLTAGE LINE REGULATION	From V_{IN}MAX to V_{IN}MIN; 100%I_{OUT}.	-0.5	-	0.5	%
OUTPUT VOLTAGE LOAD REGULATION	From 100%I_{OUT} to 10%I_{OUT}.	-0.5	-	0.5	%
EFFICIENCY	100%I_{OUT}.	55	65	-	%
HIPOT	1,12,13,24 to 10,11,14,15; 0.5mA MAX, ramp 1s,dwell 1s.	500	-	-	V_{DC}
WEIGHT		-	9.3	-	g

Figure 3: TEST CIRCUIT

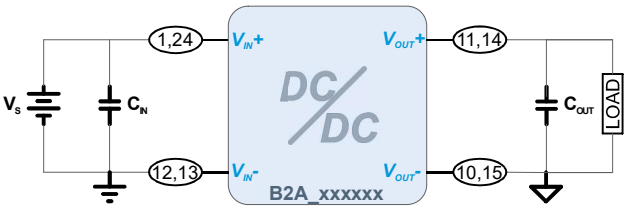
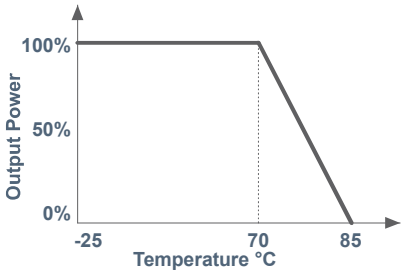


Figure 4: DERATING CURVE



NOTES:

1) C_{IN}, C_{OUT} are optional.